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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/674,444	10/31/2000	Symon Reuben Brewer	20251-000100	9030

7590 03/29/2005

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EXAMINER	
VARTANIAN, HARRY	

ART UNIT	PAPER NUMBER
2634	

DATE MAILED: 03/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/674,444	BREWER, SYMON REUBEN	
	Examiner	Art Unit	
	Harry Vartanian	2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 October 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5-12 and 15-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5-12 and 15-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 October 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-3, 5-12, 15-23 are pending in this case.

Response to Arguments

1. Applicant's arguments filed on 10/15/2004 have been fully considered but they are not persuasive. Applicant's main argument is that a reference clock signal that is offset by a predetermined frequency is not disclosed by Shohet. In the broadest sense, a frequency offset can mean a shift down or up from some reference or center frequency. Shohet uses a reference clock signal f_R to measure the jitter in clock signal f_j. Shohet states that f_j is a harmonic of f_R which means that one or the other frequency is "offset" by a difference in frequency(Column 3, Lines 4-9). In figure 2, it is shown that the reference is running at a higher frequency than jittered clock. This is one instant where the predetermined offset frequency limitation is met. Another is in the use of the high frequency clock f_H. Although f_H is not explicitly stated to be a reference clock, it is used as a reference clock to measure the phase difference between the jittered clock and the reference clock(Column 3, Lines 16-22). In figure 2, this phase difference measurement is δ_T.

Regarding the statement that the rejection "teaches away" from the invention is not considered germane for anticipation rejections. MPEP 2131.05 states:

> Arguments that the alleged anticipatory prior art is nonanalogous art' or teaches away from the invention' or is not recognized as solving the problem solved by the claimed invention, [are] not germane' to a rejection under section 102." Twin Disc, Inc. v. United States, 231 USPQ 417, 424 (Cl. Ct. 1986) (quoting In re Self, 671 F.2d 1344, 213 USPQ 1, 7 (CCPA 1982))

Claim Rejections - 35 USC § 102

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

1. Claims 1-2, 5, 7-9, 10-11, and 16 are rejected under 35 U.S.C. 102(b) as being anticipated by Shohet(United States Patent# 4,975,634). Regarding Claim 1, Shohet meets the following limitations of the Claim:

> forming an offset reference clock signal being offset by a predetermined frequency amount from said digital signal; **(column 4, lines 50-65), fig 1, fig 2**
>
> sampling said digital signal at sampling times determined by an integer multiple of the frequency of said offset reference clock signal, such that, in the absence of jitter and said offset by a predetermined frequency, there are a predetermined number of sampling times in each bit of said digital signal; **(column 4, lines 50-65), fig 1, fig 2**
>
> detecting occasions when the number of sampling times in any bit of said digital signal is different from said predetermined number; **Abstract**
>
> counting said occasions over a predetermined time, and **fig 1, Abstract**
>
> deriving at least one measure of jitter from said counting of said occasions. **(Column 3, Lines 50-54)**

Regarding Claim 2, Shohet meets the following limitations of the Claim:

> wherein said offset reference clock signal is formed by extracting a clock signal from said digital signal and offsetting said clock signal by said predetermined frequency. **(Column 1, lines 39-44)**

Regarding Claim 5, Shohet meets the following limitations of the Claim:

> wherein said sampling the times are at clock bit intervals being plus and minus one of said integer multiple. **Fig 2**

Regarding Claim 7, Shohet meets the following limitations of the Claim:

> wherein one of said at least one measure of jitter is obtained by counting up one value for each of said occasions representing sampling times greater than the predetermined number within a bit, counting down one value for each of said occasions representing sampling times less than the predetermined number within a bit and determining the difference between the maximum count value and the minimum count value. **Abstract; (Column 3, lines 56-60)**

Regarding Claim 8, Shohet meets the following limitations of the Claim:

> wherein one of said at least one measure of jitter is obtained by counting up one value for each of said occasions representing sampling times greater than the predetermined number within a bit, counting down one value for each of said occasions representing sampling times less than the predetermined number within a bit and determining the time difference between the first occasion of the maximum count value and the last occasion of the minimum count value. **Abstract; (Column 3, lines 56-60)**

Regarding Claim 9, Shohet meets the following limitations of the Claim:

> wherein the time difference is divided by said integer multiple and said predetermined time. **fig 2; fig 1, item 22, 24; (Column 4, Lines 11-12)**

Regarding Claims 10-11 and 16 the rejections for the Claims above meet the limitations of the Claims.

Claim Rejections - 35 USC § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

2. Claim 6, 15, 17, 19-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shohet. Shohet meets all the limitations of Claims 6 and 15(see above paragraphs) except disclosing the method of determining a sampling period disclosed in Claims 6 and in the last limitation of Claim 15. However, using the inverse proportion of the bit rate and higher frequency offset is a design choice and simply represents using the original clock frequency(bit rate) and some offset.

Regarding Claims 17 and 19-23, the 102 rejections for the Claims above meet the limitations of the Claims.

3. Claims 3, 12, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shohet in view of Yoshimura et al(United States Patent 6,100,724). Shohet meets all the limitations of Claims 3, 12, and 18(see above paragraphs) except disclosing the smoothing of the reference clock.

However, Yoshimura discloses:

"a phase comparator 5 for calculating a phase difference by using sampled values before and after an edge portion of the signals outputted from the A/D converter 4, ***a filter 6 for smoothing the phase difference outputted from the phase comparator 5 so as to output a signal converted into a direct current, a variable frequency oscillator 7 for reproducing a synchronous clock on the basis of the signal outputted from the filter 6, a jitter measuring section 9 for detecting a jitter detection*** signal on the basis of unevenness of the phase difference obtained by the phase comparator 5..."**(Column 3, Lines 12-24)**

Therefor is would have been prima facie obvious to smooth the reference clock. The motivation to combine is that it is well known in the art that smoothing a clock can result in more accurate phase measurements, therefor improving the jitter measurement.

Conclusion

2. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Harry Vartanian whose telephone number is 571.272.3048. The examiner can normally be reached on 10:00-6:30 Mondays to Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on 571.272.3056. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Harry Vartanian
Examiner
Art Unit 2634

HV

STEPHEN CHIN
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